REMARKS

Reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1-13 are pending in this case. Claims 1 and 8 are amended herein. Claims 14-16 are cancelled as they are drawn to a non-elected invention.

The Examiner rejected claims 1-3, 7 under 35 U.S.C. § 102(b) as being anticipated by Ishii (U.S. 5,422,307). Claim 1 is amended to overcome the rejection.

Applicant respectfully submits that amended claim 1 is unanticipated by Ishii as there is no disclosure or suggestion in Ishii of etching a metal stack and a layer of resistor material using a first pattern to form a plurality of metal lines in addition to and separate from a thin film resistor area. Ishii teaches forming a resistor by depositing a layer of resistor material and a metal stack, using a first pattern to etch the metal stack and resistor layer, and using a second pattern to etch the metal stack from over a high resistance area of the resistor layer. This leaves peripheral wiring at the ends of the resistor. There is no disclosure or suggestion in Ishii of forming a plurality of metal lines in addition to and separate from the resistor area. The only wiring taught by Ishii is the peripheral wiring of the resistor itself. No additional wiring it taught or suggested. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are unanticipated by Ishii.

The Examiner rejected claim 6 under 35 U.S.C. § 103(a) as being unpatentable over Ishii as applied to claim 1, and further in view of Morris (U.S. 5,485,138).

Applicant respectfully submits that claim 6 is patentable over Ishii in view of Morris as there is no disclosure or suggestion in the references of etching a metal stack and a layer of resistor material using a first pattern to form a plurality of metal lines in addition to and separate from a thin film resistor area, as required by claim 1 from which claim 6 depends. Morris is applied to teach vias in a dielectric layer. As discussed above, Ishii fails to teach or suggest forming the additional metal lines. The references as combined fail to suggest etching a metal stack and a layer of resistor material using a first pattern to form a plurality of metal lines in addition to and separate from a thin film resistor area. Accordingly, Applicant respectfully submits that claim 6 is patentable over the references.

The Examiner rejected claims 8-10, 12, 13 under 35 U.S.C. § 103(a) as being unpatentable over Ishii, Linn, and Morris. Claim 8 is amended to more clearly overcome the rejection.

Applicant respectfully submits that claim 8 is patentable over the combined references as there is no disclosure or suggestion in the references of dry etching a metal stack and a layer of resistor material using a first pattern to form a plurality of metal lines in addition to and separate from the thin film resistor. Ishil teaches forming a resistor by depositing a layer of resistor material and a metal stack, using a first pattern to etch the metal stack and resistor layer, and using a second pattern to etch the metal stack from over a high resistance area of the resistor layer. This leaves peripheral wiring at the ends of the resistor. The only wiring taught by Ishii is the peripheral wiring of the resistor itself. No additional wiring it taught or suggested. Morris is applied to teach vias. Lynn is applied to teach the desire to etch the metal without affecting the resistor material. There is no disclosure or suggestion in the combined references of forming a thin film resistor and a plurality of metal lines in addition to and separate from the resistor from the same metal stack. Accordingly, Applicant

respectfully submits that claim 8 and the claims dependent thereon are patentable over the references.

The Examiner rejected claims 4, 5, 11 under 35 U.S.C. § 103(a) as being unpatentable over Ishii or Ishii/Linn/Morris as applied to claim 1 and 8, and further in view of admitted prior art.

Applicant respectfully submits that claims 4, 5, and 11 are patentable over the references for the same reasons discussed above relative to claims 1 and 8, from which these claims depend. The admitted prior art is applied to teach the use of a hardmask as a pattern for etching. The combined references do not disclose or suggest forming metal lines in addition to the resistor from the same metal stack as the resistor. Accordingly, Applicant respectfully submits that claims 4, 5, and 11 are patentable over the references.

The Examiner required restriction between claims 1-13 of group I and claims 14-16 of group II. Applicant hereby affirms the provisional election of group I, claims 1-13. Claims 14-16 are accordingly, cancelled.

The other references cited by the Examiner have been reviewed, but are not felt to come within the scope of the claims as amended.

Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made.**"

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1-13. If the Examiner has any questions or other correspondence regarding this application, Applicant requests

that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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Version with Markings to Show Changes Made

Claim 1 is amended as follows:

1. (amended) A method of fabricating an integrated circuit, comprising the steps of:

forming a first interlevel dielectric over a semiconductor body;

forming a layer of resistor material over said first interlevel dielectric layer;

forming a metal stack on said layer of resistor material;

forming a first pattern over said metal stack;

etching said metal stack and said layer of resistor material using said first pattern to form a plurality of metal lines in addition to and separate from a thin film resistor area;

removing said first pattern;

forming a second pattern to expose a portion of said metal stack over [a] the thin film resistor area;

removing said exposed portion of said metal stack to form a thin film resistor.

Claim 8 is amended as follows:

8. (amended) A method of fabricating a thin film resistor in an integrated circuit, comprising the steps of:

providing a semiconductor body having a first interlevel dielectric layer;

forming a layer of resistor material over said first interlevel dielectric layer;

forming a metal stack on said layer of resistor material;

forming a first pattern over said metal stack, said first pattern covering said metal stack where a plurality of metal lines and said thin film resistor are desired;

dry etching said metal stack and said layer of resistor material using said first pattern to form said plurality of metal lines in addition to and separate from said thin film resistor;

removing said first pattern;

forming a second pattern to expose a portion of said metal stack over a thin film resistor area;

removing said exposed portion of said metal stack using a wet etch to form said thin film resistor;

removing said second pattern; and

forming a second interlevel dielectric layer over said plurality of metal lines and said thin film resistor.

Claims 14-16 are cancelled.